REMARKS

Claims 1-9, 11-14, 16-23 are currently pending in the present application. No new matter has been added. Reexamination and reconsideration of the application are respectfully requested.

REJECTION OF CLAIMS 1-23 UNDER 35 U.S.C. 103(a)

Claims 1-23 are rejected under 35 U.S.C. 103(a) for the reasons set forth on pages 2-4 of the Action. Specifically, claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walsh et al. (U.S. Pat. No. 5,870,617, hereinafter referred to as "Walsh" or "the Walsh reference") in view of Hidehiko et al. (JP 06052070A, hereinafter referred to as "Hidehiko" or "the Hidehiko reference").

The Action refers to element 920B and col. 8, lines 42-48 of Walsh as teaching the constant power area as claimed. Also, the Action refers to the system 100 and col. 8, lines 42-48 of Walsh as teaching the switched power area as claimed. Further, the Action refers to the element 920B as teaching the inactive state power reduction manager as claimed. Moreover, the Action refers to col. 13, lines 13-17 for teaching the at least one transistor that is manufactured with a sub-micron semiconductor manufacturing process as claimed.

It is respectfully submitted that element 920B does not fairly teach or suggest the inactive state power reduction manager as claimed. First, element 920B of Walsh does not perform the same function or operation as the inactive state power reduction manager as claimed. For example, col. 8, lines 42-48 states that element 920B during a 0-volt suspend mode stores "system information to either a hard disk or other non-

volatile memory array." The storing of system information does not fairly teach or suggest, "performing a scan-based state-save by employing the scan circuitry," as claimed. Since Walsh is silent as to the use of test circuitry for this step of storing, the "system information" can only fairly be interpreted as software variables (e.g., operating system variables and application program variables). This interpretation is supported by col. 88, lines 38-39 that refers to resuming an application program after exiting the suspend mode.

Furthermore, Walsh teaches that the system information is stored to either a hard disk or other non-volatile memory. Although Walsh does not appear to teach a specific manner in which this store step is performed, a typical access to a peripheral requires a call to the operating system, which in turn interfaces with device driver software that handles a read or write access to the storage device. For example, FIG. 6, HDD 122 and PPU 110 with related description support the above interpretation.

Moreover, since the PPU of Walsh performs a different function than the inactive state power reduction manager as claimed, it follows that the construction of PPU of Walsh is also very different from the power reduction manager as claimed.

The Action states that Walsh et al. does not teach the state save being a scan-based state save. Hidehiko is cited for teaching a scan-based state-save and restore of data. The Action then states "it would have been obvious to a person of ordinary skill in the art at the time of the invention to use a scan-based state-save as the state save in Walsh because this would have provided a fast method of data evacuation."

The rejections under 35 U.S.C. 103 are respectfully traversed, at least insofar as applied to the claims, and reconsideration and reexamination of the application is respectfully requested for the reasons set forth hereinbelow. Specifically, this combination is contested as improper for the reasons advanced below. Moreover, even if this combination were proper, which is not conceded, the resulting combination would still fail to teach or suggest the claimed invention.

EVEN IF PROPERLY COMBINED, THE WALSH REFERENCE AND HIDEHIKO REFERENCE FAIL TO TEACH OR SUGGEST THE SPECIFIC LIMITATIONS SET FORTH BY THE INDEPENDENT AND DEPENDENT CLAIMS

As advanced hereinbelow, the cited references are improperly combined. However, it is respectfully submitted that even if the Walsh reference and Hidehiko reference were properly combined, which is not conceded, Walsh, whether alone or in combination with Hidehiko, fails to teach or suggest specific limitations recited by the claims.

Specifically, Walsh, whether alone or in combination with Hidehiko, fails to teach or suggest "an inactive state power reduction manager .. for receiving a sleep signal and responsive thereto for asserting a stop clock signal to stop a normal mode clock, for performing a scan-based state-save", "b) stopping a normal mode clock; c) performing a state save by employing the scan circuitry," and "an inactive state power reduction manager .. for receiving a sleep signal and responsive thereto for asserting a stop clock signal to stop a normal mode clock, for performing a scan-based state save of state information of the first integrated circuit and the second integrated circuit by using

the test access port of the first integrated circuit and the second integrated circuit," as claimed in claims 1, 13, and 18, respectively.

The element 920B of Walsh does not fairly teach or suggest the inactive state power reduction manager as claimed because element 920B has a different structure and operates in a very different manner than the inactive state power reduction manager as claimed. For example, the element 920B does not perform a state save in the manner as claimed since Walsh appears to utilize software calls (e.g., operating system) to perform a state save. As described in the Background of the current application (page 4, lines 5-8), there are significant drawbacks to relying on software to perform the state save.

Furthermore although Walsh notes in passing that its circuits may be manufactured with a submicron CMOS process, Walsh fails to indicate the problem of submicron processes identified by the current application, but instead states, "a low-voltage, submicron CMOS process is utilized to achieve low system power consumption while operating at PCI clock rates up to 33 MHz and higher." Also, Walsh appears to use a "power-down mode [that] allows host software to reduce power consumption further while preserving internal register contents and allowing PC cards to interrupt the host," which is very different from the scan-based power saving techniques of the claimed invention.

Moreover, it is noted that the dependent claims incorporate all the limitations of independent claims 1, 13, and 18, respectively. Furthermore, the dependent claims

also add additional limitations, thereby making the dependent claims a fortiori and independently patentable over the cited references.

For example, dependent claims 21-23 recite limitations related to receiving a wake-up signal; responsive to the wake-up signal, re-connecting the switched power portion of the circuit to power; g) performing a state restore by employing the scan circuitry; and h) re-starting the normal mode clock. These limitations do not appear to be taught or suggested by the Walsh and Hidehiko references.

In view of the foregoing, it is respectfully submitted that the Walsh reference, whether alone or in combination with the Hidehiko reference, fails to teach or suggest the circuit, method and circuit board as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

THE PROPOSED COMBINATION IS BASED ON IMPERMISSIBLE USE OF THE CLAIMED INVENTION AS A TEMPLATE TO PIECE TOGETHER THE TEACHINGS OF THE WALSH REFERENCE AND THE HIDEHIKO REFERENCE

It is respectfully submitted that the Walsh and Hidehiko references are improperly combined. It appears that the Action uses improper hindsight to selectively pick teachings from Walsh and teachings from Hidehiko to arrive at the claimed invention.

Walsh appears to be directed to an integrated circuit that includes, "on a single chip, distinct supply voltage terminals and internal on-chip supply conductors connected respectively thereto, including a ground terminal and terminals for first and second supply voltages, and a terminal for a selectable supply voltage and also has a power-good terminal." The IC has a "plurality of peripheral control circuits connected by an on-chip internal bus." Moreover, "the peripheral control circuits connect to

different ones of the internal on-chip supply conductors for operation on the first and second supply voltages, and the selectable supply voltage." The Walsh circuit also includes reset circuitry and a control latch with a bit to which the reset circuitry is responsive. The reset circuitry provides resets for the at least one of the peripheral control circuits as a function of a voltage at the power-good terminal.

In contrast, Hidehiko is directed to an apparatus for protecting data loss. In further contrast, the invention as claimed provides power reduction management to address the problem of computing devices with transistors, manufactured with sub-micron processes, where it is no longer sufficient to simply stop the clock, but the chips must be completely disconnected from the power supply in order to conserve power as set forth in the specification. (Specification, pages 3-4) Walsh fails to address this problem.

Consequently, it appears that the current patent application has been improperly used as a basis for the motivation to combine or modify the components selected from Walsh and Hidehiko to arrive at the claimed invention. Stated differently, the proposed combination of the cited references appears to be based on impermissible hindsight reconstruction.

The Federal Circuit has held, "It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated, "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (quoting In re Fine, 837 F.2d 1071,

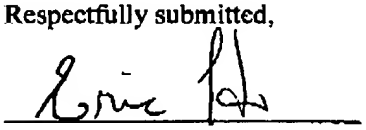
1075, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988)), In re Fritch, 23 USPQ 2d 1780, 1784 (Fed. Cir. 1992). [emphasis added.]

In view of the foregoing, it is respectfully submitted that the Walsh reference, whether alone or in combination with the Hidchiko reference, fails to teach or suggest the circuit, method, and circuit board as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

Conclusion

For all the reasons advanced above, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the pending claims are requested, and allowance is earnestly solicited at an early date. The Examiner is invited to telephone the undersigned if the Examiner has any suggestions, thoughts or comments, which might expedite the prosecution of this case.

Respectfully submitted,



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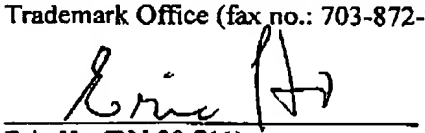

Eric Ho (RN 39,711) June 13, 2005 (Date)